WHAT IS CLAIMED IS:

1. A semiconductor device having terminal electrodes arranged, in plan view, outside a region where semiconductor chips are arranged, comprising:

a lower semiconductor chip located to overlap in the range of height with said terminal electrodes;

an upper semiconductor chip located above said lower semiconductor chip;

a wire connecting said upper and lower semiconductor chips to said terminal electrodes; and

an encapsulating resin encapsulating said upper and lower semiconductor chips and said wire,

said encapsulating resin and said terminal electrodes having respective bottom surfaces coplanar with each other.

2. The semiconductor device according to claim 1, wherein

said upper semiconductor chip is supported by a die pad portion coplanar with said terminal electrodes and

said lower semiconductor chip is arranged without overlapping in plan view with said die pad portion.

3. The semiconductor device according to claim 1, wherein

said lower semiconductor chip and said encapsulating resin have respective bottom surfaces coplanar with each other and the bottom surface of said lower semiconductor chip is exposed from said encapsulating resin.

4. The semiconductor device according to claim 1, wherein

said upper semiconductor chip is supported by a die pad portion located higher than said terminal electrodes, and said lower semiconductor chip has its bottom surface encapsulated by said encapsulating resin.

5. The semiconductor device according to claim 1, wherein

said semiconductor device is of QFN (Quad Flat Non-Lead Package) type having said terminal electrodes arranged outside to surround said semiconductor chips.

6. The semiconductor device according to claim 1, wherein said upper and lower semiconductor chips are rectangles respectively in shape, connection terminals of the semiconductor chips are arranged along shorter sides opposing each other of said rectangles, and said upper and lower semiconductor chips being rectangles in shape are arranged to cross each other in plan view.

7. The semiconductor device according to claim 1, wherein said terminal electrodes arranged outside are leads arranged along two opposing sides with said semiconductor chips therebetween.

8. A semiconductor device of TSOP (Thin Small Outline Package) type having semiconductor chips arranged between a first lead portion and a second lead portion provided respectively on two sides opposing in plan view, comprising:

a first die pad portion integrated with and noncoplanar with said first lead portion and located higher relative to a reference plane passing through central position between the highest surface and the lowest surface of said first and second lead portions;

a second die pad portion integrated with and noncoplanar with said second lead portion and located lower relative to said reference plane; and

a lower semiconductor chip supported by said first die pad portion and an upper semiconductor chip supported by said second die pad portion, said two semiconductor chips being partially overlapped and located to overlap in the range of height with said first and second lead portions.

9. The semiconductor device according to claim 8, wherein said first die pad portion is provided to a first lead frame located including said first lead portion above said reference plane, and

said second die pad portion is provided to a second lead frame located including said second lead portion below said reference plane.

10. The semiconductor device according to claim 9, wherein said first die pad portion is L-shaped including a first extension extending from an end of said first lead portion toward said second lead portion and a first opposing portion continuing from said first extension and extending in parallel with said first lead portion,

said second die pad portion is arranged in plan view opposite said first die pad portion and L-shaped including a second extension extending from an end of said second lead portion toward said first lead portion and a second opposing portion continuing from said second extension and extending in parallel with said second lead portion,

said first extension and said first opposing portion have their bottom surface supporting said lower semiconductor chip, and

said second extension and said second opposing portion have their upper surface supporting said upper semiconductor chip.

11. The semiconductor device according to claim 8, wherein said first and second lead portions and said first and second die pad portions are integrated into a common lead frame, said reference plane passes through center of thickness of said lead frame, said first die pad portion supports said lower semiconductor chip of said partially overlapped semiconductor chips, and said second die pad portion supports said upper semiconductor chip.

12. The semiconductor device according to claim 11, wherein center of thickness of said first die pad portion and center of thickness of said second die pad portion are spaced vertically from said reference plane in respective directions opposite to each other, each by a distance equal to the sum of a half of thickness of said lead frame and a half of thickness of an adhesive layer bonding said upper and lower semiconductor chips.

13. A method of manufacturing a semiconductor device comprising:

a lead frame stacking step of stacking a first lead frame on a second lead frame, said first lead frame including a first lead portion and a first die pad portion extending in L-shape from an end of said first lead portion along periphery of a region where a lower semiconductor chip is arranged, said second lead frame including a second lead portion and a second die pad portion opposing said first die pad portion in plan view and extending in L-shape from an end of said second lead portion along periphery of a region where an upper semiconductor chip is arranged, said first and second lead portions opposing in plan view with said upper and lower semiconductor chips therebetween;

a semiconductor chip bonding step of bonding said lower semiconductor chip to said first die pad portion and bonding said upper semiconductor chip to said second die pad portion;

a welding step of welding together said first lead frame and said second lead frame at their overlapping portion;

a wire bonding step of connecting said upper and lower semiconductor chips to a terminal electrode by a wire;

a resin encapsulating step of encapsulating by means of a resin a region inside said overlapping portion being welded; and

a cutting off step of cutting off a portion outside said resin encapsulated first and second lead portion and said upper and lower semiconductor chips in said resin encapsulating step.

14. The method of manufacturing a semiconductor device according to claim 13, wherein said lead frame stacking step and said semiconductor chip bonding step are combined and

sub steps of said lead frame stacking step and sub steps of said semiconductor chip bonding step are partially changed in their order to be performed.

15. The method of manufacturing a semiconductor device according to claim 13, wherein said lead frame stacking step and said semiconductor

chip bonding step are combined and

said lead frame stacking step and said semiconductor chip bonding step include a die bonding material arranging step of arranging a die bonding material bonding said upper and lower semiconductor chips to said first and second die pad portions.